In the Drawings:

Please replace previously submitted Figures 1A-14E with the red lined informal versions of Figures 1A-12E submitted herewith.

Figures 1A-12E show changes from the original drawings filed in the parent case.

In the Claims:

Please cancel, without prejudice, claims 4-9 and substitute the following new claims:

11. A passenger transit car comprising:

a) at least one car drive motor;

b) a first plurality of solenoids;

c) a second plurality of mechanical switches;

d) a third plurality of motors for moving doors on said passenger transit car;

e) An electrical control unit comprising:

i) a mother board having a fourth plurality of daughter boards wherein said electrical control unit is connected to said first plurality of solenoids, to said second plurality of mechanical switches, and to said third plurality of motors for moving doors on said passenger transit car;

ii) a self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

A) a non-clocked, non-inverting amplifier chip for connection to one of said bit lines;

B) a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip; and

C) wherein said self-locking memory circuit has upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds.

12. A passenger transit car according to claim 11 wherein said self-locking memory circuit includes:

a central processing unit;

a Digital Signal Processor for transceiving discrete electrical inputs; and

a tri state data bus electrically connecting said Digital Signal Processor to said central processing unit, said Digital Signal Processor and said central processing unit having different clock rates for accessing said tri state data bus.

13. A passenger transit car according to claim 11 wherein said self-locking memory circuit includes:

a Complex Programmable Logic Device for transceiving discrete electrical signals; and

wherein said tri state data bus electrically interconnects said central processing unit, said Digital Signal Processor, and said Complex Programmable Logic Device, said Digital Signal Processor and said Complex Programmable Logic Device having clock rates for accessing said tri state data bus that are different from a clock rate at which said central processing unit accesses said tri state data bus.

14. a self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein said self-locking memory circuit has upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds; and

wherein a ratio between said resistance and an output